Overview

The WSP2416 DSP core, as shown in **Figure 1**, is a high-speed scalar (one instruction per clock cycle) 24/16-bit integer Dual-mode (24-bit and 16-bit mode) Digital Signal Processor optimized for high-end audio, communications, consumer electronics, multi-media, and other high-speed signal processing applications.

The WSP2416 DSP core combines the popular ADSP-218X architecture (3 Computational Units – ALU, MULT/MAC, Shifter, a Program Sequencer, 2 Data Address Generators, 2 DMA Ports, 2 Serial Ports, a Programmable Timer, Flag I/O, General Purpose I/Os, extensive Interrupt capability, IO space registers and on-core Program Memory (PM) and Data Memory (DM)) and the patent-pending 24-bit/Special Feature Enhanced Mode, which adds full 24-bit capabilities to the standard 16-bit architecture to better serve the computational applications that are more precision-demanding as well as hooks for adding new instructions and additional banks of the Register File. Similar to the PM, the DM in the WSP2416 core is implemented with Dual-Access capability to allow both instruction and DMA triggered access to take place in the same cycle. Further, the Dual-access DM can be implemented to be partially 16-bit and partially 24-bit wide, so 24-bit data can be stored in both PM and DM in the 24-bit Mode. The control needed for the 24-bit/Special Feature Enhanced Mode is by the TFCMR (24-bit Mode Control Register) that is accessed by standard ADSP-218X instructions, thus requiring no changes to the standard ADSP-218X compiler or assembler to use the Special Features. It takes just one cycle to switch between the 24-bit and 16-bit mode or the standard and enhanced mode.

In addition to the standard ADSP-218X instructions, the WSP2416 DSP core features MIN, MAX instructions. Also included in the flexible WSP2416 architecture is an extra set of the I (Index), M (Modify), L (Length) Registers used in the Data Address Generators for more efficient context switching than the standard ADSP-218X. As a result, lower clock rate is expected using WSP2416 than ADSP-218X for the same applications and thus saving more power. Also provided in the WSP2416 DSP core is firmware programmable Phase-Lock Loop (PLL) that can be programmed during normal operations and thus change the clock rate to the DSP core "on the fly".

The WSP2416 core integrates 80K bytes of patented Dual-Access Memory implemented with single-port memory configured as 16K (x 24) of PM and 16K (x 24/16) of DM. Both PM and DM sizes can be adjusted (increased or reduced) according to the applications' needs. The overall area of the WSP2416 DSP core is very sensitive to the sizes of

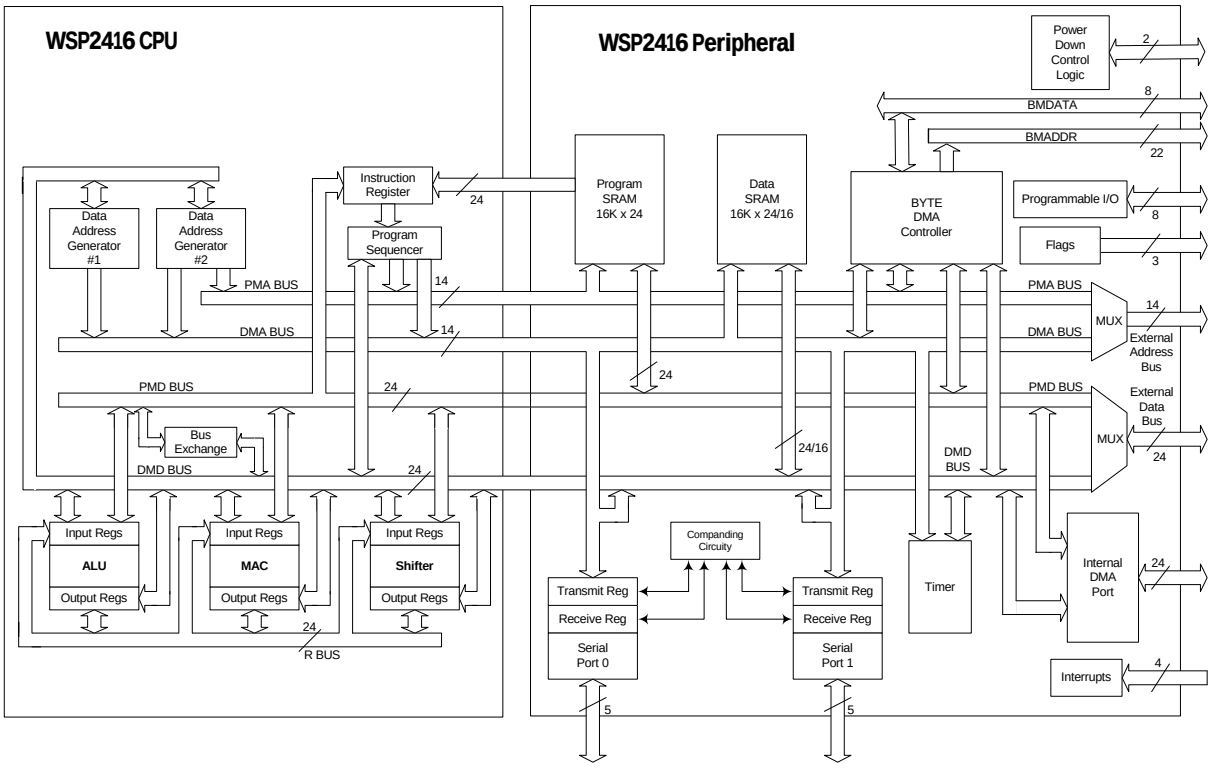

Figure 1. WSP2416 DSP Core Functional Block Diagram

the PM and DM chosen, since they are the majority of the overall WSP2416 silicon real estate. It is possible to "mix and match" ROM and SRAM for the Program and/or Data Memory to minimize the die size for fixed applications. Power-down circuitry is provided for optimum power management.

The WSP2416 core is fully synthesizeable. Its PLL, MAC, and Memory Blocks are available as hard macros in 0.35µm and 0.25µm processes for most pure-play foundries. Implementations of these hard macros in other more advanced processes are straight-forward.

The WSP2416 core has also been successfully implemented in industry's standard FPGAs.

Features Summary

- **ADSP-218X Fully Compatible Architecture**
  - Fully Compatible Instructions
  - On-Core 16Kx24 PM and 16Kx24/16 DM
  - ALU, MAC, Shifter Functional Units
  - Two Data Address Generation Units (DAG)
  - IDMA and BDMA ports
  - Single Cycle Execution
  - Zero Overhead Looping
  - Two Serial Ports
  - Programmable Timer
  - General Purpose I/Os
  - Interrupt and Power-Down
  - On-Core Programmable PLL
- **24/16-Bit Dual Mode Processor**
  - 24-bit and 16-bit Mode Dynamic Switching in Single Cycle
  - Utilizing Same ADSP-218X Assembler, Compiler, and development environment
  - Full 24-bit Functional Units
    - 24-bit ALU producing 24/16-bit results
    - 56±24x24 MAC producing 24/16-bit results
    - 48-bit Shifter producing 24/16-bit results
  - 24-bit Arithmetic Registers
  - 24-bit Internal Busses
    - 24-bit Data Bus of PM and DM
  - 24-bit External Bus
  - 24-bit IDMA Port
- **Other Enhancement**
  - Separate BDMA Port and IO Space
  - Synchronous Dual-Access PM and DM
  - One extra set of I, M, L Address Generator registers for more efficient Context Switching
  - Powerful Min, Max Instructions
  - Hooks for larger Register File
  - Instruction Set Extension
  - Easily Configurable PM and DM sizes
  - Expanded I/Os for easy embedding in SoC designs
  - Flexible Expandable 24-bit DM (any words anywhere in the DM can be 24-bit wide)
  - Dynamic Frequency Change
  - 3 Design Patents
- **Small Size and Low Power Consumption**
  - Small Core Size (~35K gates)
  - Lower Operating frequency than standard ADSP-218X for given applications
  - Flexible Power Management
- **Design Availability**
  - Fully Synthesizable Verilog Code
  - Memory blocks in 0.35µm and 0.25µm
  - PLL blocks in 0.35µm and 0.25µm
  - High-speed MAC blocks in 0.35µm and 0.25µm

Applications

With two DMA ports, and flexible boot methods, WSP2416 DSP core can be integrated with a lot of peripherals to achieve most signal-processing SoC applications.

WSP2416 is suitable for various types of real-time DSP applications; Digital Filters, One-/Two-Dimensional FFT, DCT, Linear Predictive Speech Coding, PCM, ADPCM, High-speed Modems, GSM CODEC, Image Processing, Speech Recognition, and digital music CODEC, to just name a few. Following is an example of the WSP2416 DSP core being used in the popular MP3/WMA digital music player applications. It is important to note that in this example design, as shown in **Figure 2**, almost all I/O's are General Purpose I/O's (GPIO's), which can be programmed and thus controlled individually or in group by the DSP firmware. These powerful and flexible GPIO's are used to control SMC flash memory chip & card, MMC flash memory card, SDRAM, EPP (enhanced Parallel Port) and other standard micro-controllers, like 8051 and 6811.

With the total number of GPIO's well exceeding twice of those of a typical 8051 microcontroller, it is fair to say that this design is actually an integrated DSP/micro-controller design with a unified instruction set, which is the ADSP-218X instruction set.

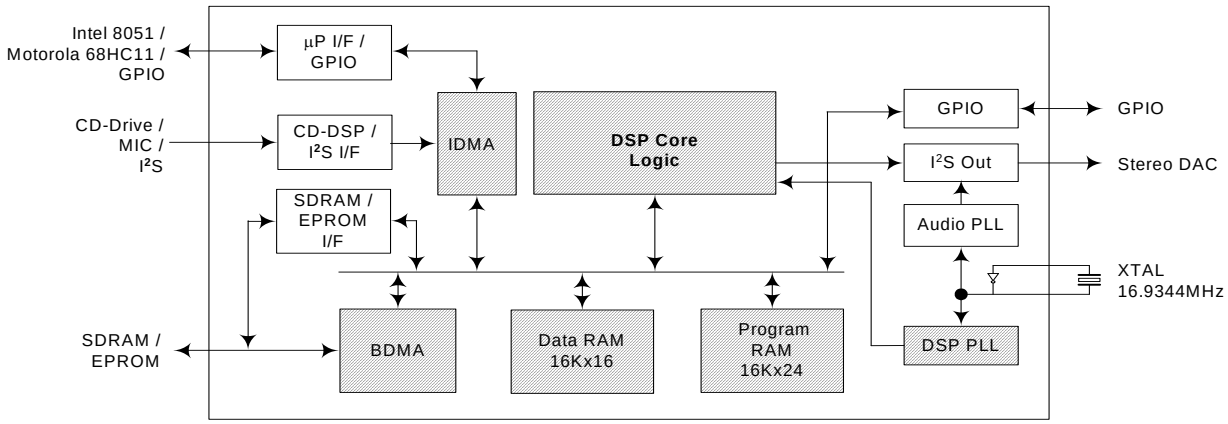

Figure 2. WSP2416 DSP Core Audio Application Diagram

WSP2416 DSP Core I/O Definition

Figure 3 shows the I/O definition of the WSP2416 core as an IP.

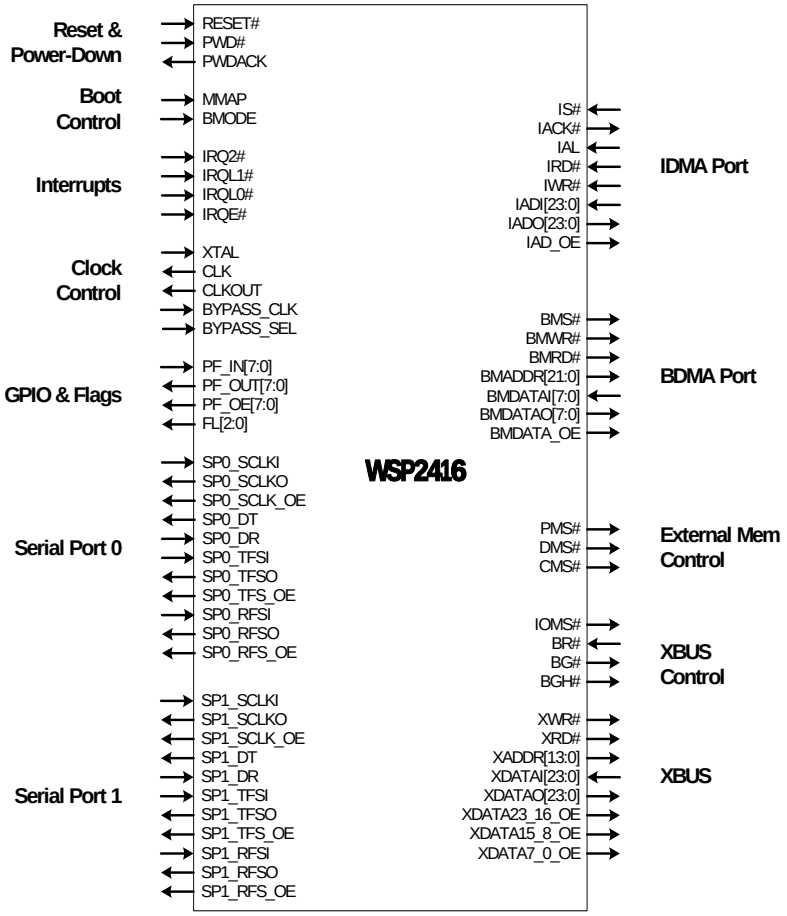

Figure 3. WSP2416 DSP Core I/O